FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-10165-3E

MEMORY

# CMOS 1 M × 16 BIT FAST PAGE MODE DYNAMIC RAM

# MB8116160A-60/-70

**CMOS 1,048,576 × 16 BIT Fast Page Mode Dynamic RAM**



## ■ DESCRIPTION

The Fujitsu MB8116160A is a fully decoded CMOS Dynamic RAM (DRAM) that contains 16,777,216 memory cells accessible in 16-bit increments. The MB8116160A features a ”fast page” mode of operation whereby high-speed random access of up to 256-bits of data within the same row can be selected. The MB8116160A DRAM is ideally suited for mainframe, buffers, hand-held computers video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB8116160A is very small, the device can be used as a non-volatile memory in equipment that uses batteries for primary and/or auxiliary power.

The MB8116160A is fabricated using silicon gate CMOS and Fujitsu’s advanced four-layer polysilicon and two-layer aluminum process. This process, coupled with advanced stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB8116160A are not critical and all inputs are TTL compatible.

## ■ PRODUCT LINE & FEATURES

| Parameter | | MB8116160A-60 | MB8116160A-70 |
|---|---|---|---|
| $\overline{RAS}$ Access Time | | 60 ns max. | 70 ns max. |
| Random Cycle Time | | 110 ns min. | 130 ns min. |
| Address Access Time | | 30 ns max. | 35 ns max. |
| $\overline{CAS}$ Access Time | | 15 ns max. | 17 ns max. |
| Fast Page Mode Cycle Time | | 40 ns min. | 45 ns min. |
| Low Power Dissipation | Operating Current | 550 mW max. | 495 mW max. |
| | Standby Current | 11 mW max. (LVTTL level) / 5.5 mW max. (CMOS level) | |

- 1,048,576 words × 16 bit organization
- Silicon gate, CMOS, Advanced Capacitor Cell
- All input and output are TTL compatible
- 4096 refresh cycles every 65.6ms
- Self refresh function
- Early write or $\overline{OE}$ controlled write capability
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast Page Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

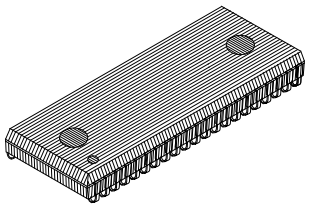
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

## ■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

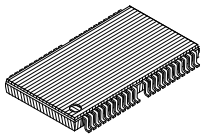
| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Voltage at any pin relative to $V_{SS}$ | $V_{IN}$, $V_{OUT}$ | –0.5 to +7.0 | V |
| Voltage of $V_{CC}$ supply relative to $V_{SS}$ | $V_{CC}$ | –0.5 to +7.0 | V |
| Power Dissipation | $P_D$ | 1.0 | W |
| Short Circuit Output Current | — | 50 | mA |
| Operating Temperature | $T_{OPE}$ | 0 to 70 | °C |
| Storage Temperature | $T_{STG}$ | –55 to +125 | °C |

**WARNING:** Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ■ PACKAGE



Plastic SOJ Package
(LCC-42P-M01)

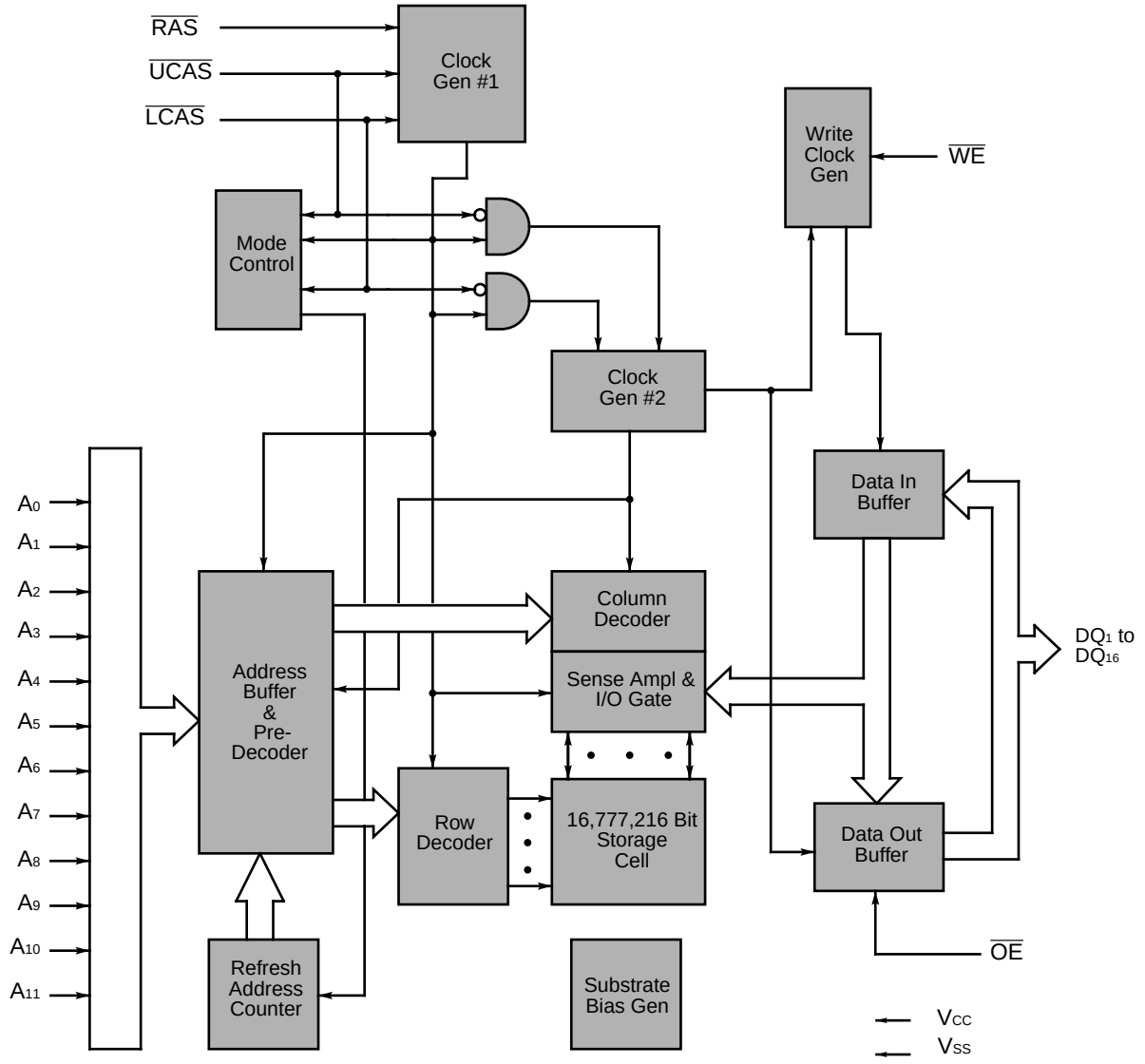


Plastic TSOP Package
(FPT-50P-M06)
(Normal Bend)

**Package and Ordering Information**

– 42-pin plastic (400mil) SOJ, order as MB8116160A-××PJ
– 50-pin plastic (400mil) TSOP-II with normal bend leads, order as MB8116160A-××PFTN

**Fig. 1 – MB8116160A DYNAMIC RAM – BLOCK DIAGRAM**




## ■ CAPACITANCE

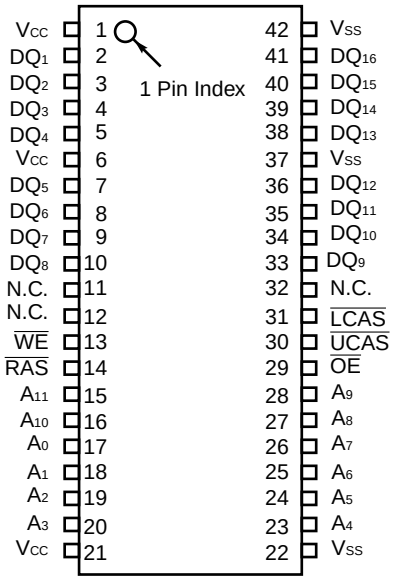
($T_A$=25°C, f = 1MHz)

| Parameter | Symbol | Max. | Unit |
|---|---|---|---|
| Input Capacitance, $A_0$ to $A_{11}$ | $C_{IN1}$ | 5 | pF |
| Input Capacitance, $\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$ | $C_{IN2}$ | 5 | pF |
| Input/Output Capacitance, $DQ_1$ to $DQ_{16}$ | $C_{DQ}$ | 7 | pF |

## ■ PIN ASSIGNMENTS AND DESCRIPTIONS

**42-Pin SOJ**

(TOP VIEW)

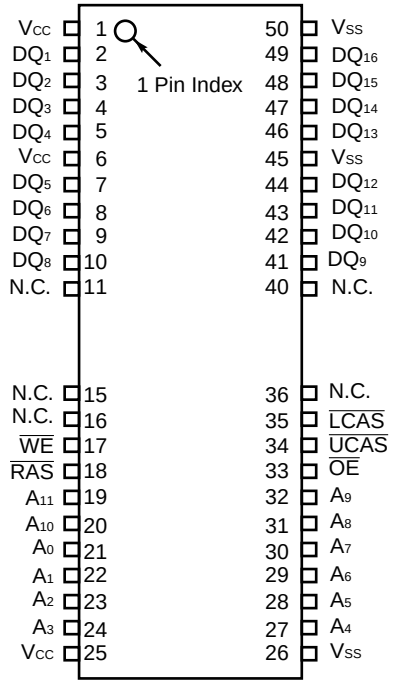



| Designator | Function |
|---|---|
| $A_0$ to $A_{11}$ | Address inputs<br>row : $A_0$ to $A_{11}$<br>column : $A_0$ to $A_7$<br>refresh : $A_0$ to $A_{11}$ |
| $\overline{RAS}$ | Row address strobe |
| $\overline{LCAS}$ | Lower column address strobe |
| $\overline{UCAS}$ | Upper column address strobe |
| $\overline{WE}$ | Write enable |
| $\overline{OE}$ | Output enable |
| $DQ_1$ to $DQ_{16}$ | Data Input/Output |
| $V_{CC}$ | +5.0 volt power supply |
| $V_{SS}$ | Circuit ground |
| N.C. | No connection |

**50-Pin TSOP**

(TOP VIEW)

<Normal Bend>



## ■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Notes | Symbol | Min. | Typ. | Max. | Unit | Ambient Operating Temp. |
|---|---|---|---|---|---|---|---|
| Supply Voltage | 1 | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 0°C to + 70°C |
| | | $V_{SS}$ | 0 | 0 | 0 | | |
| Input High Voltage, all inputs | 1 | $V_{IH}$ | 2.4 | — | 6.5 | V | |
| Input Low Voltage, all inputs* | 1 | $V_{IL}$ | –3.0 | — | 0.8 | V | |

* : Undershoots of up to –2.0 volts with a pulse width not exceeding 20 ns are acceptable.

## ■ FUNCTIONAL OPERATION

### ADDRESS INPUTS

Twenty input bits are required to decode any sixteen of 16,777,216 cell addresses in the memory matrix. Since only twelve address bits (A0 to A11) are available, the column and row inputs are separately strobed by $\overline{LCAS}$ or $\overline{UCAS}$ and $\overline{RAS}$ as shown in Figure 1. First, twelve row address bits are input on pins A0-through-A11 and latched with the row address strobe ($\overline{RAS}$) then, eight column address bits are input and latched with the column address strobe ($\overline{LCAS}$ or $\overline{UCAS}$). Both row and column addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{LCAS}$ or $\overline{UCAS}$, respectively. The address latches are of the flow-through type; thus, address information appearing after $t_{RAH}$ (min) + $t_T$ is automatically treated as the column address.

### WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

### DATA INPUT

Input data is written into memory in either of three basic ways-an early write cycle, an $\overline{OE}$ (delayed) write cycle, and a read-modify-write cycle. The falling edge of $\overline{WE}$ or $\overline{LCAS}$ / $\overline{UCAS}$, whichever is later, serves as the input data-latch strobe. In an early write cycle, the input data of DQ1-DQ8 is strobed by $\overline{LCAS}$ and DQ9-DQ16 is strobed by $\overline{UCAS}$ and the setup/hold times are referenced to each $\overline{LCAS}$ and $\overline{UCAS}$ because $\overline{WE}$ goes Low before $\overline{LCAS}$ / $\overline{UCAS}$. in a delayed write or a read-modify-write cycle, $\overline{WE}$ goes Low after $\overline{LCAS}$ / $\overline{UCAS}$; thus, input data is strobed by $\overline{WE}$ and all setup/hold times are referenced to the write-enable signa

### DATA OUTPUT

The three-state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs are obtained under the following conditions:

- $t_{RAC}$ : from the falling edge of $\overline{RAS}$ when $t_{RCD}$ (max) is satisfied.
- $t_{CAC}$ : from the falling edge of $\overline{LCAS}$ (for DQ1-DQ8) $\overline{UCAS}$ (for DQ9-DQ16) when $t_{RCD}$ is greater than $t_{RCD}$ (max).
- $t_{AA}$ : from column address input when $t_{RAD}$ is greater than $t_{RAD}$ (max).
- $t_{OEA}$ : from the falling edge of $\overline{OE}$ when $\overline{OE}$ is brought Low after $t_{RAC}$, $t_{CAC}$, or $t_{AA}$, and $t_{RCD}$ (max) is satisfied.

The data remains valid until either $\overline{LCAS}$ / $\overline{UCAS}$ or $\overline{OE}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high-impedance state during the entire cycle.

### FAST PAGE MODE OF OPERATION

The fast page mode of operation provides faster memory access and lower power dissipation. The fast page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions, $\overline{RAS}$ is held Low for all contiguous memory cycles in which row addresses are common. For each fast page of memory, any of 256x16-bits can be accessed and, when multiple MB8116160As are used, $\overline{CAS}$ is decoded to select the desired memory fast page. Fast page mode operations need not be addressed sequentially and combinations of read, write, and/or read-modify-write cycles are permitted.

## ■ DC CHARACTERISTICS

**(Recommended operating conditions unless otherwise noted.) Note 3**

| Parameter | Notes | Symbol | Condition | Values | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Output high voltage | 1 | $V_{OH}$ | $I_{OH}$ = –5.0 mA | 2.4 | — | — | V |
| Output low voltage | 1 | $V_{OL}$ | $I_{OL}$ = +4.2 mA | — | — | 0.4 | V |
| Input leakage current (any input) | | $I_{I(L)}$ | 0 V ≤ $V_{IN}$ ≤ $V_{CC}$; 4.5 V ≤ $V_{CC}$ ≤ 5.5 V; $V_{SS}$ = 0 V; All other pins not under test = 0 V | –10 | — | 10 | µA |
| Output leakage current | | $I_{DQ(L)}$ | 0V≤ $V_{OUT}$ ≤ $V_{CC}$; Data out disabled | –10 | — | 10 | µA |
| Operating current (Average power supply current) 2 | MB8116160A-60 | $I_{CC1}$ | $\overline{RAS}$ & $\overline{LCAS}$, $\overline{UCAS}$ cycling; $t_{RC}$ = min | — | — | 100 | mA |
| | MB8116160A-70 | | | | | 90 | mA |
| Standby current (Power supply current) | TTL level | $I_{CC2}$ | $\overline{RAS}$ = $\overline{LCAS}$, $\overline{UCAS}$ = $V_{IH}$ | — | — | 2.0 | mA |
| | CMOS level | | $\overline{RAS}$ = $\overline{LCAS}$, $\overline{UCAS}$ ≥ $V_{CC}$ – 0.2 V | | | 1.0 | mA |
| Refresh current #1 (Average power supply current) 2 | MB8116160A-60 | $I_{CC3}$ | $\overline{LCAS}$, $\overline{UCAS}$ = $V_{IH}$, $\overline{RAS}$ cycling; $t_{RC}$ = min | — | — | 100 | mA |
| | MB8116160A-70 | | | | | 90 | mA |
| Fast Page Mode Current 2 | MB8116160A-60 | $I_{CC4}$ | $\overline{RAS}$ = $V_{IL}$, $\overline{LCAS}$, $\overline{UCAS}$ cycling; $t_{PC}$ = min | — | — | 90 | mA |
| | MB8116160A-70 | | | | | 80 | mA |
| Refresh current #2 (Average power supply current) 2 | MB8116160A-60 | $I_{CC5}$ | $\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; $t_{RC}$ = min | — | — | 90 | mA |
| | MB8116160A-70 | | | | | 80 | mA |
| Refresh current #3 (Average power supply current) | MB8116160A-60 | $I_{CC9}$ | $\overline{RAS}$ = $V_{IL}$, $\overline{CAS}$ = $V_{IL}$ Self refresh; $t_{RASS}$ = min | — | — | 1000 | µA |
| | MB8116160A-70 | | | | | | |

## ■ AC CHARACTERISTICS

**(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5**

| No. | Parameter | Notes | Symbol | MB8116160A-60 | | MB8116160A-70 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | |
| 1 | Time Between Refresh | | $t_{REF}$ | — | 65.6 | — | 65.6 | ms |
| 2 | Random Read/Write Cycle Time | | $t_{RC}$ | 110 | — | 130 | — | ns |
| 3 | Read-Modify-Write Cycle Time | | $t_{RWC}$ | 150 | — | 174 | — | ns |
| 4 | Access Time from $\overline{RAS}$ | 6, 9 | $t_{RAC}$ | — | 60 | — | 70 | ns |
| 5 | Access Time from $\overline{CAS}$ | 7, 9 | $t_{CAC}$ | — | 15 | — | 17 | ns |
| 6 | Column Address Access Time | 8, 9 | $t_{AA}$ | — | 30 | — | 35 | ns |
| 7 | Output Hold Time | | $t_{OH}$ | 3 | — | 3 | — | ns |
| 8 | Output Buffer Turn On Delay Time | | $t_{ON}$ | 0 | — | 0 | — | ns |
| 9 | Output Buffer Turn Off Delay Time | 10 | $t_{OFF}$ | — | 15 | — | 17 | ns |
| 10 | Transition Time | | $t_T$ | 3 | 50 | 3 | 50 | ns |
| 11 | $\overline{RAS}$ Precharge Time | | $t_{RP}$ | 40 | — | 50 | — | ns |
| 12 | $\overline{RAS}$ Pulse Width | | $t_{RAS}$ | 60 | 100000 | 70 | 100000 | ns |
| 13 | $\overline{RAS}$ Hold Time | | $t_{RSH}$ | 15 | — | 17 | — | ns |
| 14 | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | | $t_{CRP}$ | 5 | — | 5 | — | ns |
| 15 | $\overline{RAS}$ to $\overline{CAS}$ Delay Time | 11, 12 | $t_{RCD}$ | 20 | 45 | 20 | 53 | ns |
| 16 | $\overline{CAS}$ Pulse Width | | $t_{CAS}$ | 15 | — | 17 | — | ns |
| 17 | $\overline{CAS}$ Hold Time | | $t_{CSH}$ | 60 | — | 70 | — | ns |
| 18 | $\overline{CAS}$ Precharge Time (Normal) | 19 | $t_{CPN}$ | 10 | — | 10 | — | ns |
| 19 | Row Address Set Up Time | | $t_{ASR}$ | 0 | — | 0 | — | ns |
| 20 | Row Address Hold Time | | $t_{RAH}$ | 10 | — | 10 | — | ns |
| 21 | Column Address Set Up Time | | $t_{ASC}$ | 0 | — | 0 | — | ns |
| 22 | Column Address Hold Time | | $t_{CAH}$ | 15 | — | 15 | — | ns |
| 23 | Column Address Hold Time from $\overline{RAS}$ | | $t_{AR}$ | 35 | — | 35 | — | ns |
| 24 | $\overline{RAS}$ to Column Address Delay Time | 13 | $t_{RAD}$ | 15 | 30 | 15 | 35 | ns |
| 25 | Column Address to $\overline{RAS}$ Lead Time | | $t_{RAL}$ | 30 | — | 35 | — | ns |
| 26 | Column Address to $\overline{CAS}$ Lead Time | | $t_{CAL}$ | 30 | — | 35 | — | ns |
| 27 | Read Command Set Up Time | | $t_{RCS}$ | 0 | — | 0 | — | ns |
| 28 | Read Command Hold Time Referenced to $\overline{RAS}$ | 14 | $t_{RRH}$ | 0 | — | 0 | — | ns |
| 29 | Read Command Hold Time Referenced to $\overline{CAS}$ | 14 | $t_{RCH}$ | 0 | — | 0 | — | ns |
| 30 | Write Command Set Up Time | 15, 20 | $t_{WCS}$ | 0 | — | 0 | — | ns |
| 31 | Write Command Hold Time | | $t_{WCH}$ | 15 | — | 15 | — | ns |

## ■ AC CHARACTERISTICS (Continued)

**(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5**

| No. | Parameter | Notes | Symbol | MB8116160A-60 | | MB8116160A-70 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | |
| 32 | Write Hold Time from $\overline{RAS}$ | | $t_{WCR}$ | 35 | — | 35 | — | ns |
| 33 | $\overline{WE}$ Pulse Width | | $t_{WP}$ | 15 | — | 15 | — | ns |
| 34 | Write Command to $\overline{RAS}$ Lead Time | | $t_{RWL}$ | 15 | — | 17 | — | ns |
| 35 | Write Command to $\overline{CAS}$ Lead Time | | $t_{CWL}$ | 15 | — | 17 | — | ns |
| 36 | DIN Set Up Time | | $t_{DS}$ | 0 | — | 0 | — | ns |
| 37 | DIN Hold Time | | $t_{DH}$ | 15 | — | 15 | — | ns |
| 38 | Data Hold Time from $\overline{RAS}$ | | $t_{DHR}$ | 35 | | 35 | | ns |
| 39 | $\overline{RAS}$ to $\overline{WE}$ Delay Time | 20 | $t_{RWD}$ | 80 | — | 92 | — | ns |
| 40 | $\overline{CAS}$ to $\overline{WE}$ Delay Time | 20 | $t_{CWD}$ | 35 | — | 39 | — | ns |
| 41 | Column Address to $\overline{WE}$ Lead Time | 20 | $t_{AWD}$ | 50 | — | 57 | — | ns |
| 42 | $\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh cycles) | | $t_{RPC}$ | 5 | — | 5 | — | ns |
| 43 | $\overline{CAS}$ Set Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh | | $t_{CSR}$ | 0 | — | 0 | — | ns |
| 44 | $\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh | | $t_{CHR}$ | 10 | — | 12 | — | ns |
| 45 | Access Time from $\overline{OE}$ | 9 | $t_{OEA}$ | — | 15 | — | 17 | ns |
| 46 | Output Buffer Turn Off Delay from $\overline{OE}$ | 10 | $t_{OEZ}$ | — | 15 | — | 17 | ns |
| 47 | $\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data | | $t_{OEL}$ | 10 | — | 10 | — | ns |
| 48 | $\overline{OE}$ Hold Time Referenced to $\overline{WE}$ | 16 | $t_{OEH}$ | 5 | — | 5 | — | ns |
| 49 | $\overline{OE}$ to Data In Delay Time | | $t_{OED}$ | 15 | — | 17 | — | ns |
| 50 | $\overline{CAS}$ to Data In Delay Time | | $t_{CDD}$ | 15 | — | 17 | — | ns |
| 51 | DIN to $\overline{CAS}$ Delay Time | 17 | $t_{DZC}$ | 0 | — | 0 | — | ns |
| 52 | DIN to $\overline{OE}$ Delay Time | 17 | $t_{DZO}$ | 0 | — | 0 | — | ns |
| 60 | Fast Page Mode $\overline{RAS}$ Pulse width | | $t_{RASP}$ | — | 100000 | — | 100000 | ns |
| 61 | Fast Page Mode Read/WriteCycle Time | | $t_{PC}$ | 40 | — | 45 | — | ns |
| 62 | Fast Page Mode Read-Modify-Write Cycle Time | | $t_{PRWC}$ | 80 | — | 89 | — | ns |
| 63 | Access Time from $\overline{CAS}$ Precharge | 9, 18 | $t_{CPA}$ | — | 35 | — | 40 | ns |
| 64 | Fast Page Mode $\overline{CAS}$ Precharge Time | | $t_{CP}$ | 10 | — | 10 | — | ns |
| 65 | Fast Page Mode $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge | | $t_{RHCP}$ | 35 | — | 40 | — | ns |
| 66 | Fast Page Mode $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time | | $t_{CPWD}$ | 55 | — | 62 | — | ns |

Notes:
1. Referenced to $V_{SS}$.
2. $I_{CC}$ depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   $I_{CC}$ depends on the number of address change as $\overline{RAS} = V_{IL}$, $\overline{UCAS} = V_{IH}$, $\overline{LCAS} = V_{IH}$ and $V_{IL} > -0.3$ V.
   $I_{CC1}$, $I_{CC3}$, $I_{CC4}$ and $I_{CC5}$ are specified at one time of address change during $\overline{RAS} = V_{IL}$ and $\overline{UCAS} = V_{IH}$, $\overline{LCAS} = V_{IH}$.
   $I_{CC2}$ is specified during $\overline{RAS} = V_{IH}$ and $V_{IL} > -0.3$ V.
3. An initial pause ($\overline{RAS} = \overline{CAS} = V_{IH}$) of 200 µs is required after power-up followed by any eight $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume $t_T = 5$ ns.
5. $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring timing of input signals. Also transition times are measured between $V_{IH}$ (min) and $V_{IL}$ (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If $t_{RCD}$ is greater than the maximum recommended value shown in this table, $t_{RAC}$ will be increased by the amount that $t_{RCD}$ exceeds the value shown. Refer to Fig.2 and 3.
7. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is $t_{CAC}$.
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is $t_{AA}$.
9. Measured with a load equivalent to two TTL loads and 50 pF.
10. $t_{OFF}$ and $t_{OEZ}$ is specified that output buffer change to high impedance state.
11. Operation within the $t_{RCD}$ (max) limit ensures that $t_{RAC}$ (max) can be met. $t_{RCD}$ (max) is specified as a reference point only; if $t_{RCD}$ is greater than the specified $t_{RCD}$ (max) limit, access time is controlled exclusively by $t_{CAC}$ or $t_{AA}$.
12. $t_{RCD}$ (min) = $t_{RAH}$ (min) + 2 $t_T$ + $t_{ASC}$ (min).
13. Operation within the $t_{RAD}$ (max) limit ensures that $t_{RAC}$ (max) can be met. $t_{RAD}$ (max) is specified as a reference point only; if $t_{RAD}$ is greater than the specified $t_{RAD}$ (max) limit, access time is controlled exclusively by $t_{CAC}$ or $t_{AA}$.
14. Either $t_{RRH}$ or $t_{RCH}$ must be satisfied for a read cycle.
15. $t_{WCS}$ is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.
16. Assumes that $t_{WCS} < t_{WCS}$ (min).
17. Either $t_{DZC}$ or $t_{DZO}$ must be satisfied.
18. $t_{CPA}$ is access time from the selection of a new column address (that is caused by changing $\overline{UCAS}$ and $\overline{LCAS}$ from "L" to "H"). Therefore, if $t_{CP}$ is long, $t_{CPA}$ is longer than $t_{CPA}$ (max).
19. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh.
20. $t_{WCS}$, $t_{CWD}$, $t_{RWD}$, $t_{AWD}$ and $t_{CPWD}$ are not restrictive operating parameters. They are included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and $D_{OUT}$ pin will maintain high impedance state through-out the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPWD} \geq t_{CPWD}$ (min), the cycle is a read-modify-write cycle and data from the selected cell will appear at the $D_{OUT}$ pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the $D_{OUT}$ pin, and write operation can be executed by satisfying $t_{RWL}$, $t_{CWL}$, and $t_{RAL}$ specifications.

**Fig. 2 – $t_{RAC}$ vs. $t_{RCD}$**

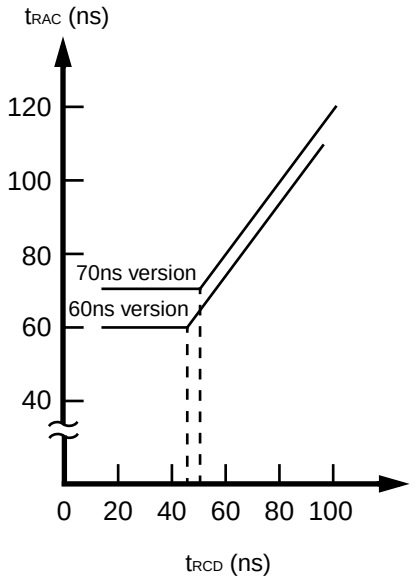



**Fig. 3 – $t_{RAC}$ vs. $t_{RAD}$**

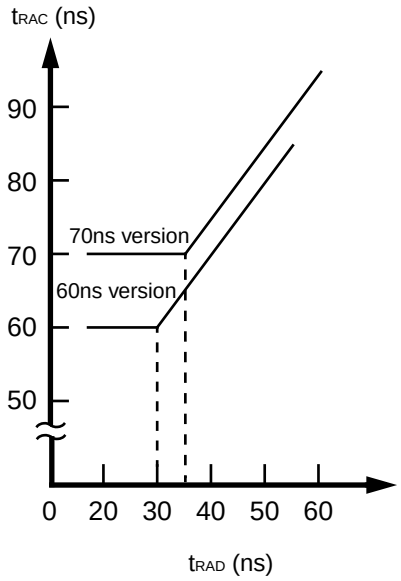
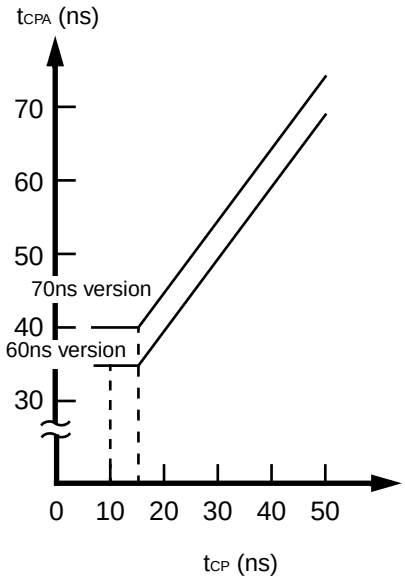



**Fig. 4 – $t_{CPA}$ vs. $t_{CP}$**

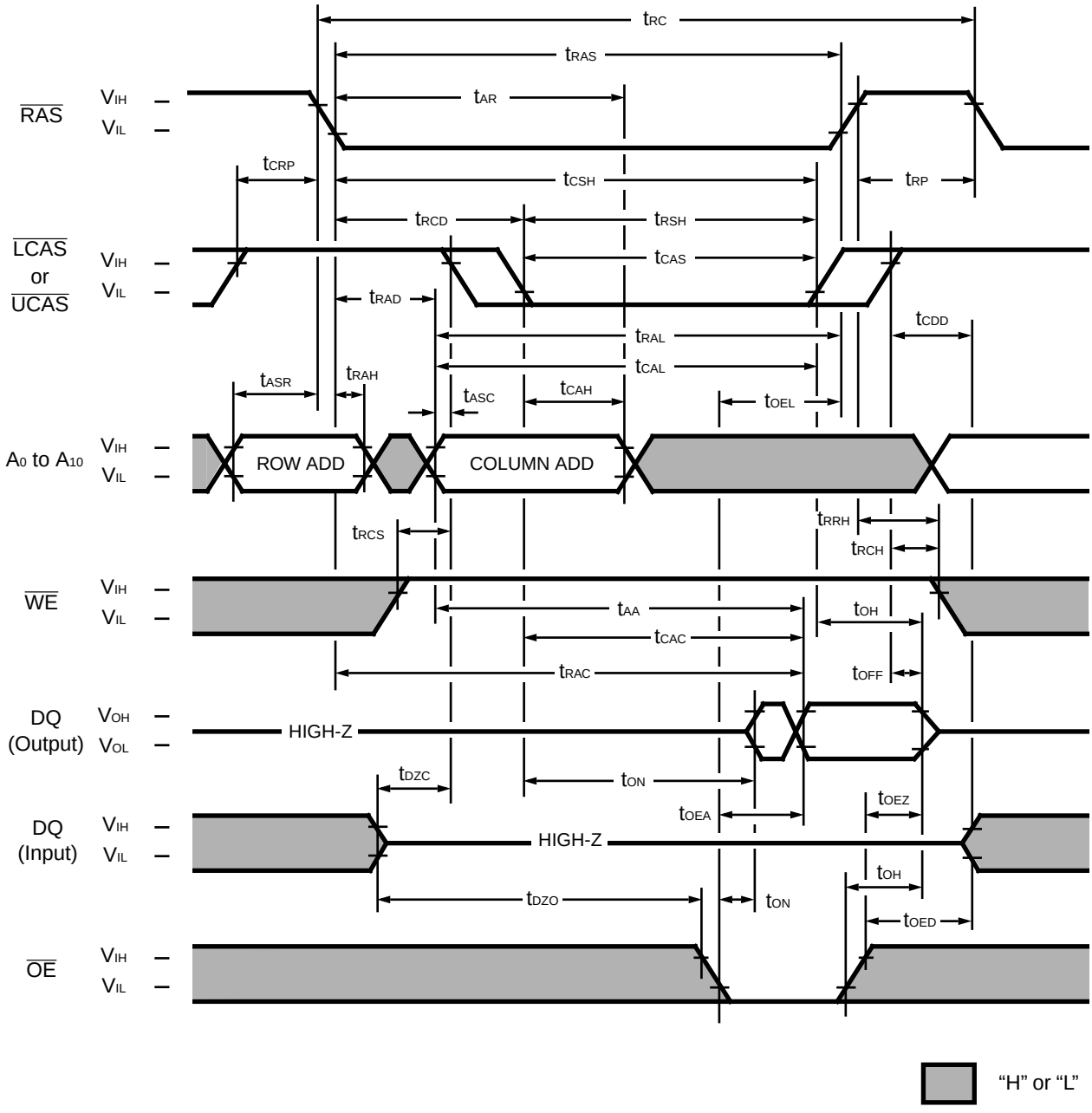



## ■ FUNCTIONAL TRUTH TABLE

| Operation Mode | Clock Input | | | | | Address | | Input/Output Data | | | | Refresh | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | $DQ_1$ to $DQ_8$ | | $DQ_9$ to $DQ_{16}$ | | | |
| | $\overline{RAS}$ | $\overline{LCAS}$ | $\overline{UCAS}$ | $\overline{WE}$ | $\overline{OE}$ | Row | Column | Input | Output | Input | Output | | |
| Standby | H | H | H | X | X | — | — | — | High-Z | — | High-Z | — | |
| Read Cycle | L | L<br>H<br>L | H<br>L<br>L | H | L | Valid | Valid | — | Valid<br>High-Z<br>Valid | — | High-Z<br>Valid<br>Valid | Yes* | $t_{RCS} \geq t_{RCS}$ (min) |
| Write Cycle (Early Write) | L | L<br>H<br>L | H<br>L<br>L | L | X | Valid | Valid | Valid<br>—<br>Valid | High-Z | —<br>Valid<br>Valid | High-Z | Yes* | $t_{WCS} \geq t_{WCS}$ (min) |
| Read-Modify-Write Cycle | L | L<br>H<br>L | H<br>L<br>L | H→L | L→H | Valid | Valid | Valid<br>—<br>Valid | Valid<br>High-Z<br>Valid | —<br>Valid<br>Valid | High-Z<br>Valid<br>Valid | Yes* | |
| $\overline{RAS}$-only Refresh Cycle | L | H | H | X | X | Valid | — | — | High-Z | — | High-Z | Yes* | |
| $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle | L | L | L | X | X | — | — | — | High-Z | — | High-Z | Yes | $t_{CSR} \geq t_{CSR}$ (min) |
| Hidden Refresh Cycle | H→L | L<br>H<br>L | H<br>L<br>L | H→X | L | — | — | — | Valid<br>High-Z<br>Valid | — | High-Z<br>Valid<br>Valid | Yes | Previous data is kept. |

X; "H" or "L"
*; It is impossible in Fast Page Mode.

**Fig. 5 – READ CYCLE**



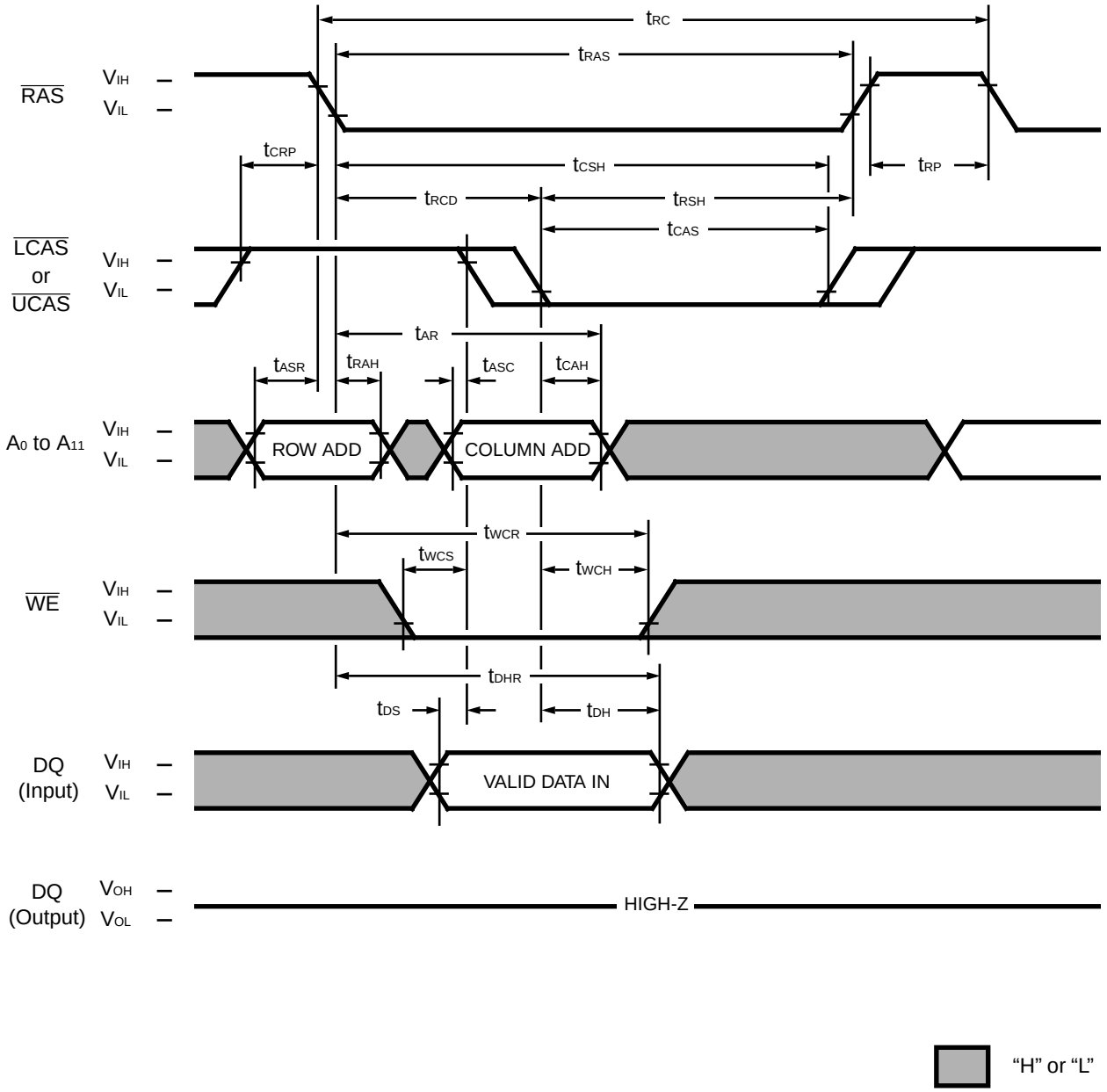

**DESCRIPTION**

To implement a read operation, a valid address is latched by the $\overline{RAS}$ and $\overline{LCAS}$ or $\overline{UCAS}$ address strobes and with $\overline{WE}$ set to a High level and $\overline{OE}$ set to a low level, the output is valid once the memory access time has elapsed. $\overline{LCAS}$ controls the input/output data on DQ1-DQ8 pins, $\overline{UCAS}$ controls one on DQ8-DQ16 pins. The access time is determined by $\overline{RAS}$($t_{RAC}$), $\overline{LCAS}$/$\overline{UCAS}$($t_{CAC}$), $\overline{OE}$($t_{OEA}$) or column addresses ($t_{AA}$) under the following conditions:

If $t_{RCD} > t_{RCD}$ (max), access time = $t_{CAC}$.
If $t_{RAD} > t_{RAD}$ (max), access time = $t_{AA}$.
If $\overline{OE}$ is brought Low after $t_{RAC}$, $t_{CAC}$, or $t_{AA}$(whichever occurs later), access time = $t_{OEA}$.

However, if either $\overline{LCAS}$ / $\overline{UCAS}$ or $\overline{OE}$ goes High, the output returns to a high-impedance state after $t_{OH}$ is satisfied.

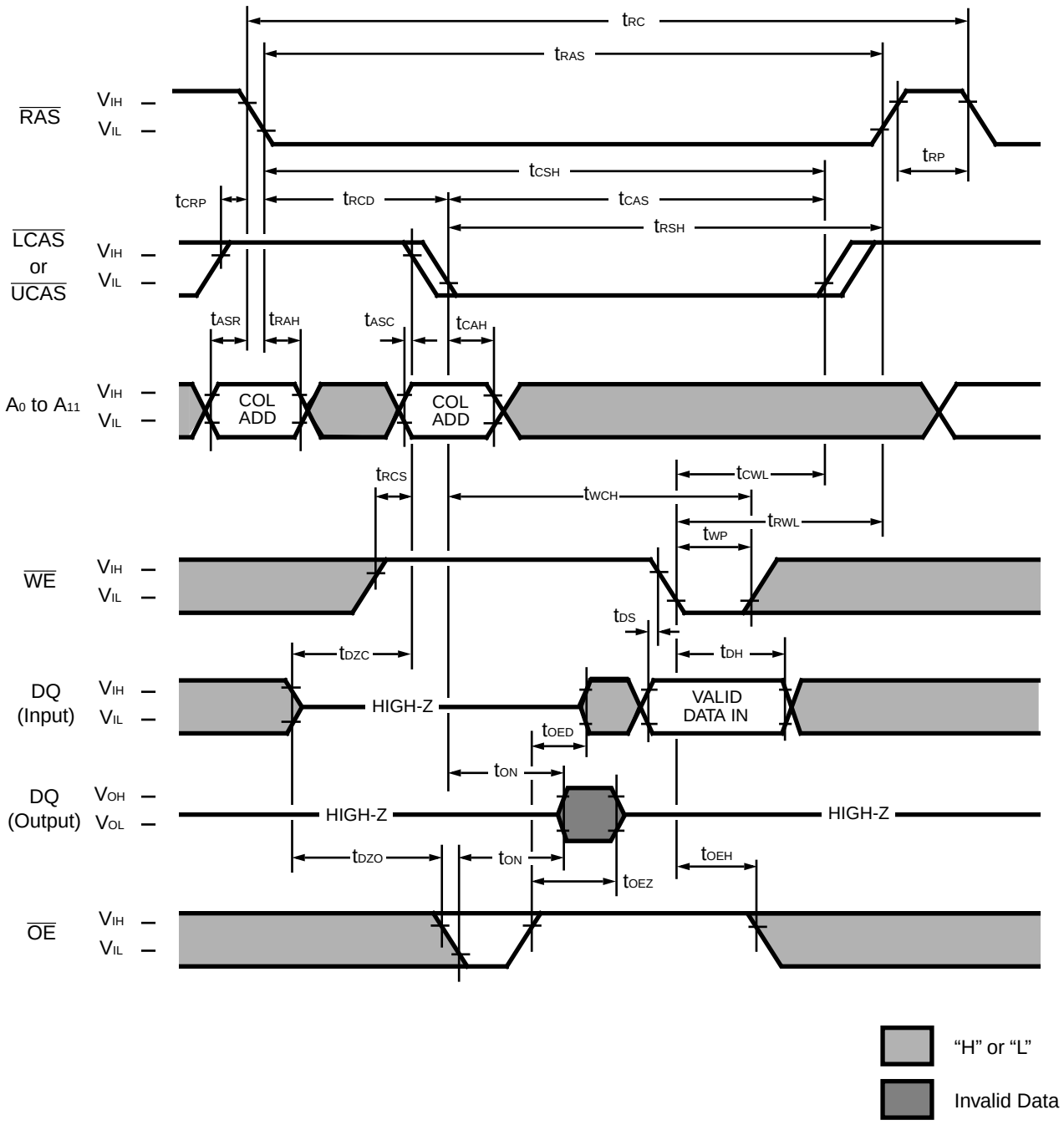
**Fig. 6 – EARLY WRITE CYCLE ($\overline{OE}$ = "H" or "L")**




**DESCRIPTION**

A write cycle is similar to a read cycle except $\overline{WE}$ is set to a Low state and $\overline{OE}$ is an "H" or "L" signal. A write cycle can be implemented in either of three ways - early write, delayed write, or read-modify-write. During all write cycles, timing parameters $t_{RWL}$, $t_{CWL}$, $t_{RAL}$ and $t_{CAL}$ must be satisfied. In the early write cycle shown above $t_{WCS}$ satisfied, data on the DQ pins are latched with the falling edge of $\overline{LCAS}$ or $\overline{UCAS}$ and written into memory.

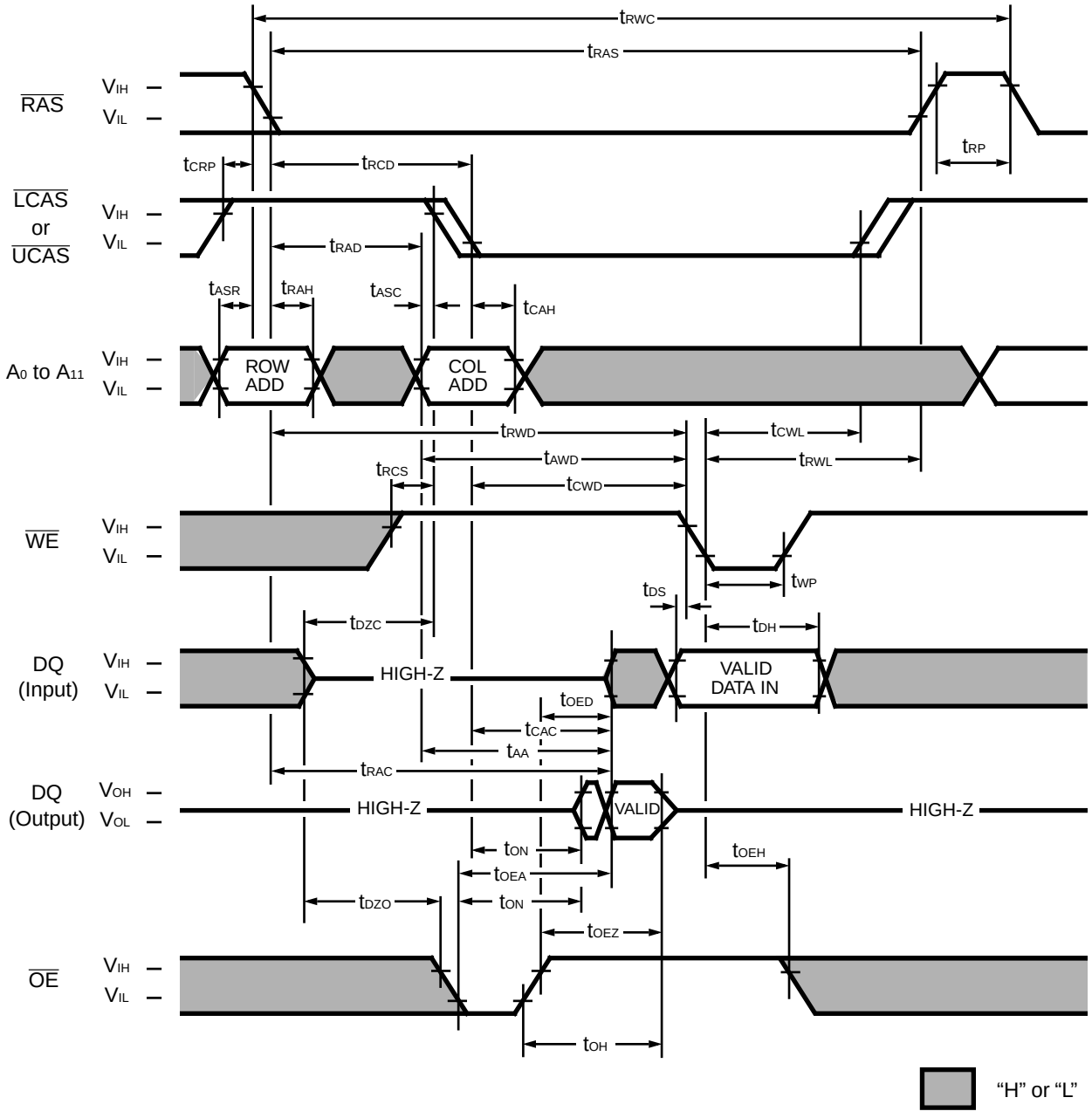
**Fig. 7 – DELAYED WRITE CYCLE**




**DESCRIPTION**

In the delayed write cycle, $t_{WCS}$ is not satisfied; thus, the data on the DQ pins is latched with the falling edge of $\overline{WE}$ and written into memory. The Output Enable ($\overline{OE}$) signal must be changed from Low to High before $\overline{WE}$ goes Low ($t_{OED} + t_T + t_{DS}$).

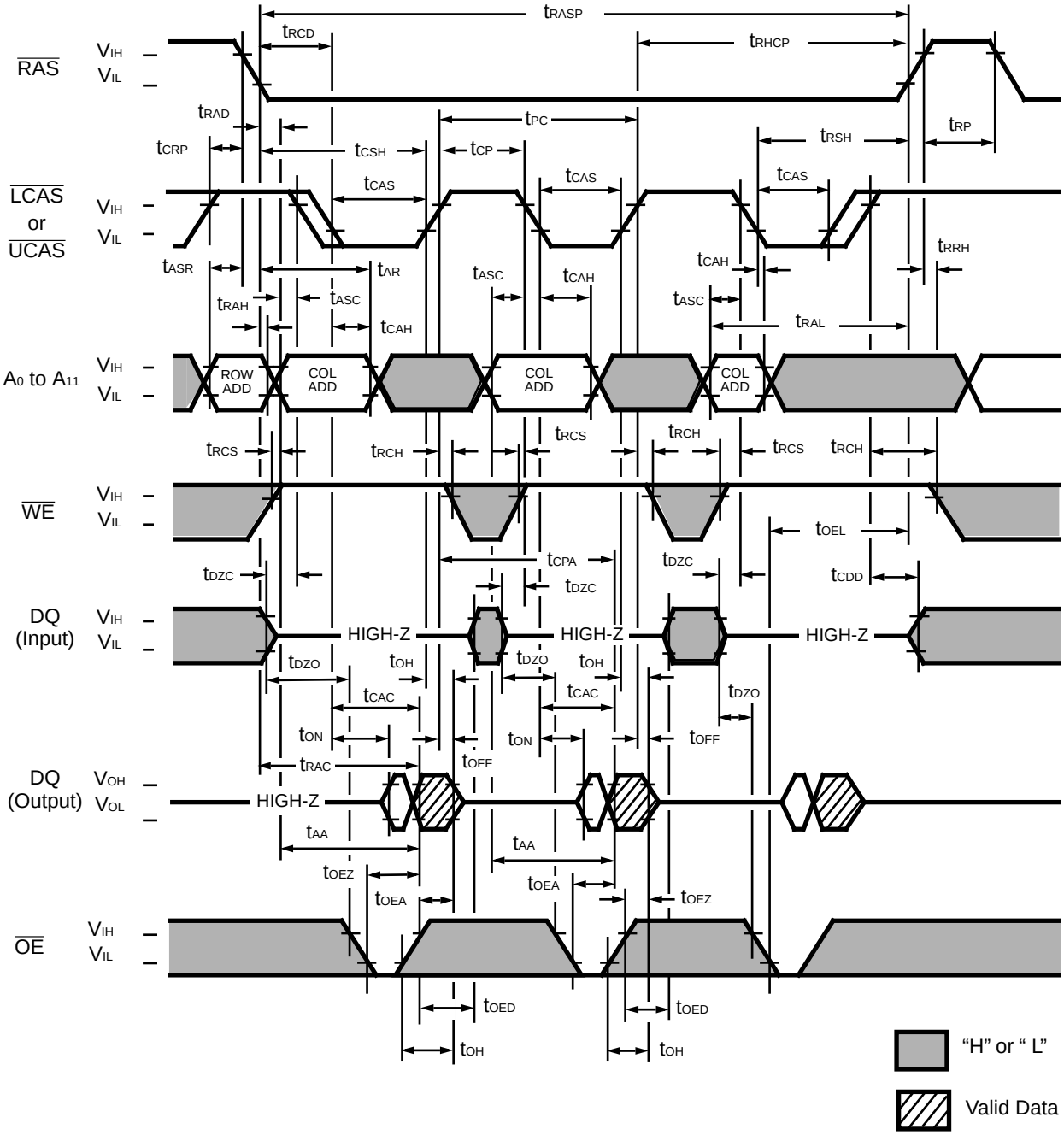
**Fig. 8 – READ-MODIFY-WRITE CYCLE**




**DESCRIPTION**

The read-modify-write cycle is executed by changing $\overline{WE}$ from High to Low after the data appears on the DQ pins. In the read-modify-write cycle, $\overline{OE}$ must be changed from Low to High after the memory access time.

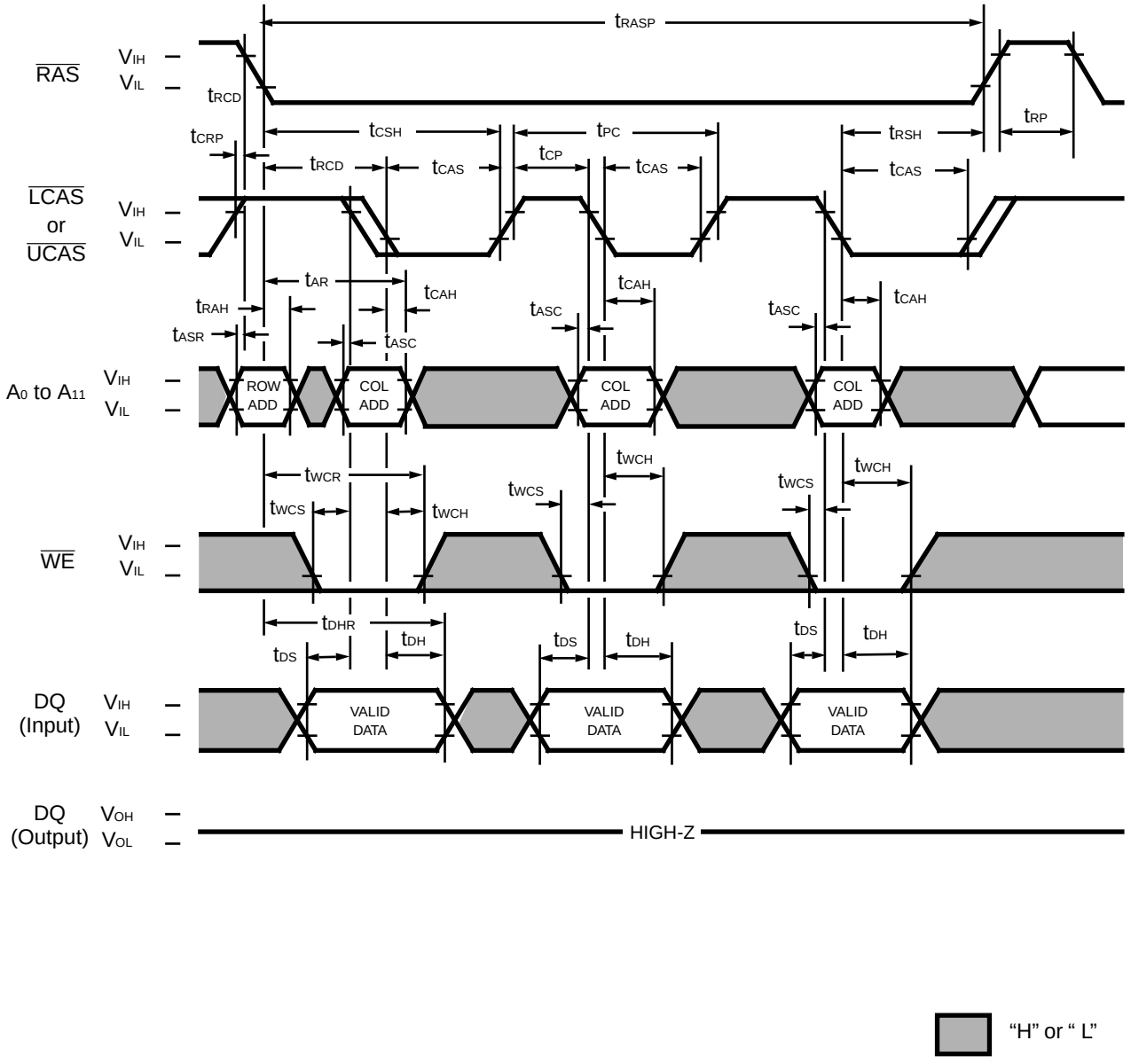
**Fig. 9 – FAST PAGE MODE READ CYCLE**




**DESCRIPTION**

The fast page mode of operation permits faster sucessive memory operations at multiple column locations of the same row address. This operations is performed by strobing in the row address and maintaining $\overline{RAS}$ at a Low level and $\overline{WE}$ at a Hight level druing all successive memory cycles in which the row address is latched. The address time is determined by $t_{CAC}$, $t_{AA}$, $t_{CPA}$, or $t_{OEA}$, which ever one is the lastest in occurring.

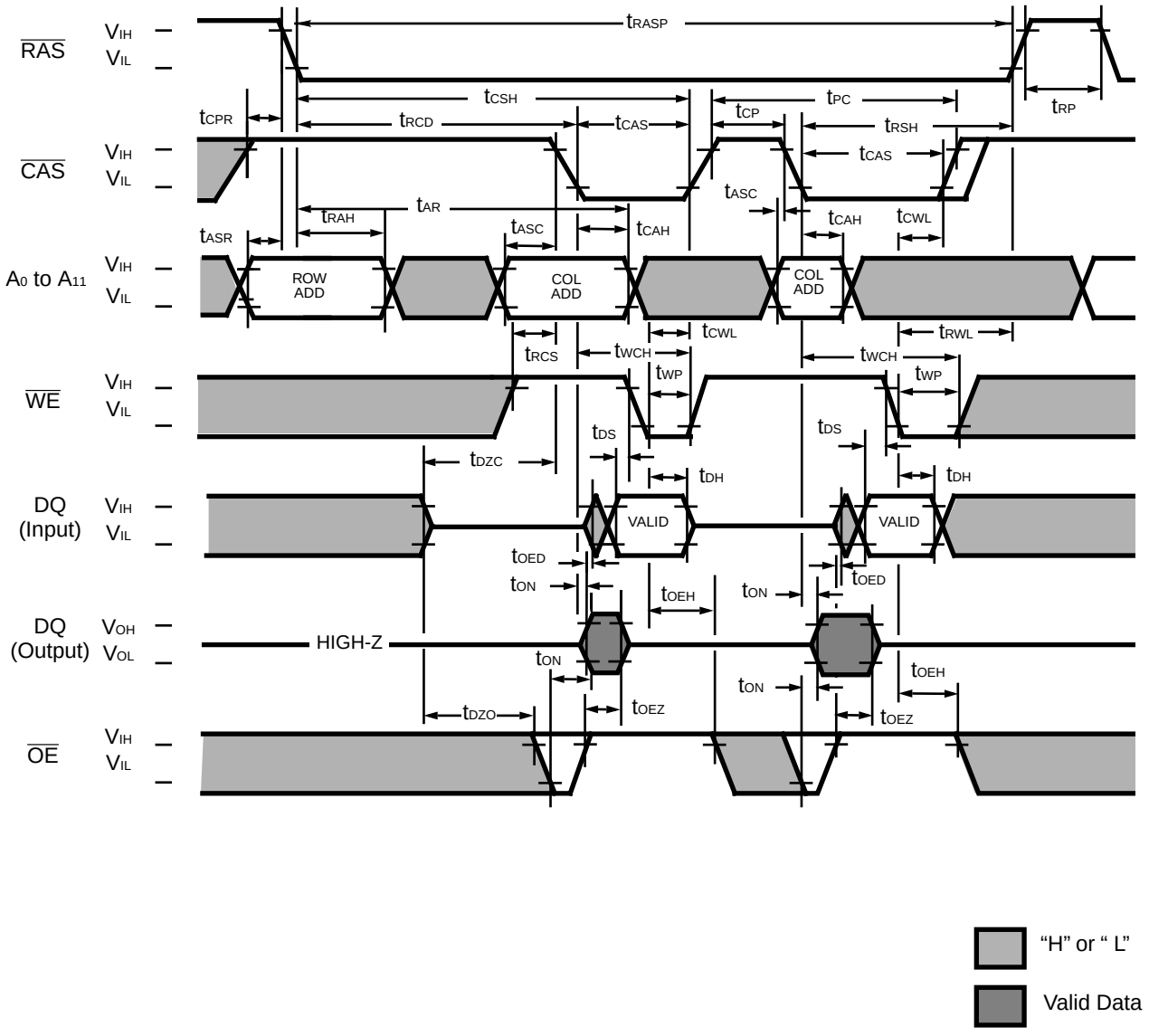
**Fig. 10 – FAST PAGE MODE EARLY WRITE CYCLE ($\overline{OE}$ = "H" or "L")**




**DESCRIPTION**

The fast page mode early write cycle is executed in the same manner as the fast page mode read cycle except the states of $\overline{WE}$ and $\overline{OE}$ are reversed. Data appearing on the DQ1 to DQ8 is latched on the falling edge of $\overline{LCAS}$ and one appearing on the DQ9 to DQ16 is latched on the falling edge of $\overline{UCAS}$ and the data is written into the memory. During the fast page mode early write cycle, including the delayed ($\overline{OE}$) write and read-modify-write cycles, $t_{CWL}$ must be satisfied.

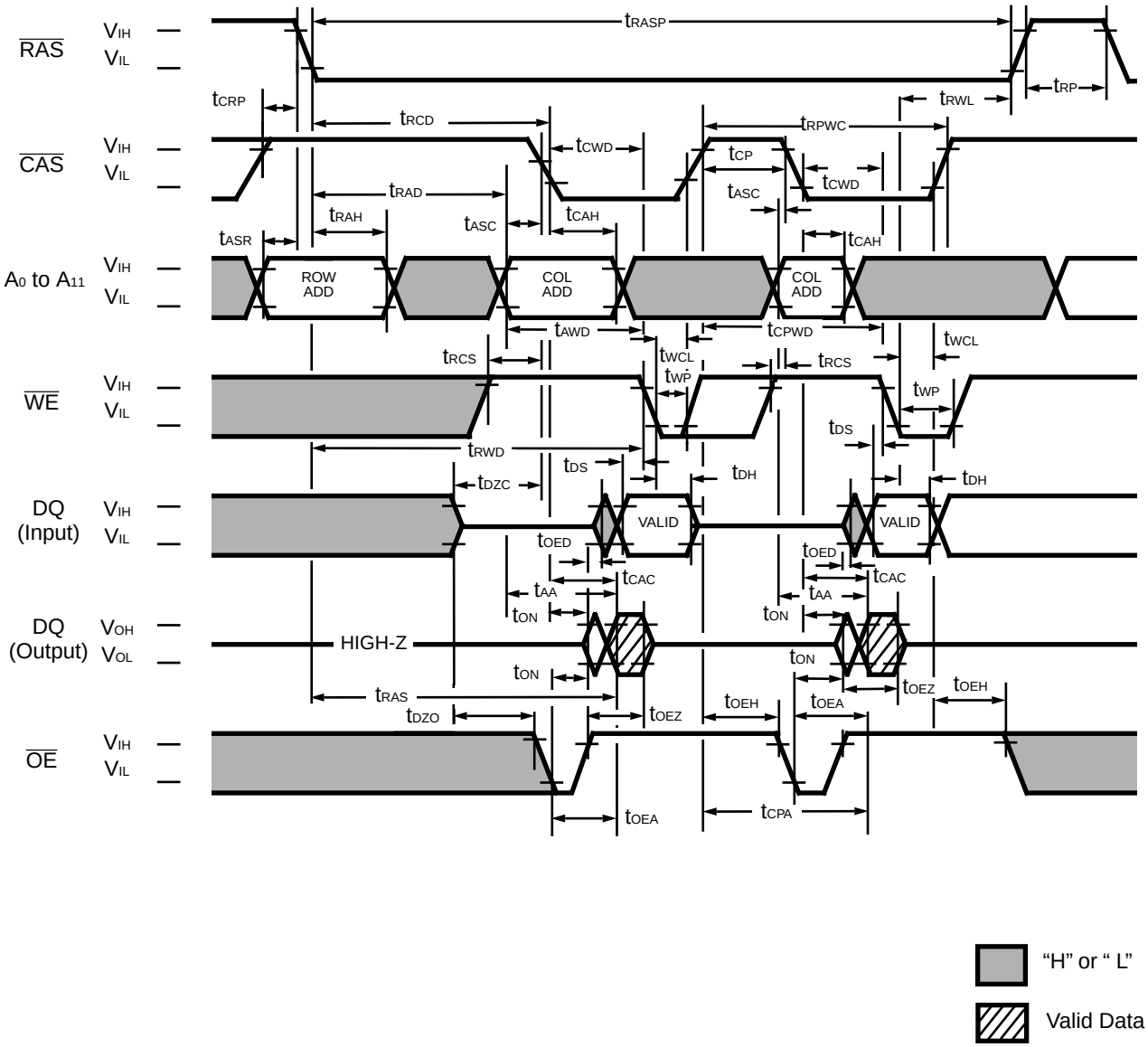
**Fig. 11 – FAST PAGE MODE DELAYED WRITE CYCLE**




**DESCRIPTION**

The fast page mode delayed write cycle is executed in the same manner as the fast page mode early write cycle except for the states of $\overline{WE}$ and $\overline{OE}$. Input data on the DQ pins are latched on the falling edge of $\overline{WE}$ and written into memory. In the fast page mode delayed write cycle, $\overline{OE}$ must me changed from Low to High before $\overline{WE}$ goes Low ($t_{OED} + t_T + t_{DS}$).

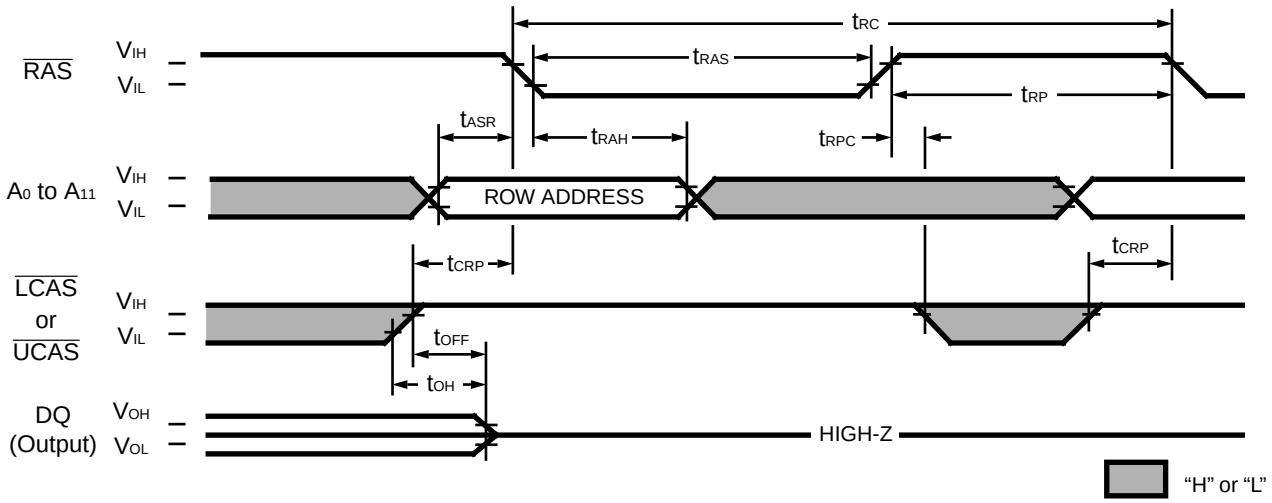
**Fig. 12 – FAST PAGE MODE READ-MODIFY-WRITE CYCLE**




**DESCRIPTION**

During the fast page mode of operation, the read-modify-write cycle can be executed by switching $\overline{WE}$ from High to Low after input data appears at the DQ pins during a normal cycle.

**Fig. 13 – $\overline{RAS}$-ONLY REFRESH ($\overline{WE}$ = $\overline{OE}$ = "H" or "L")**

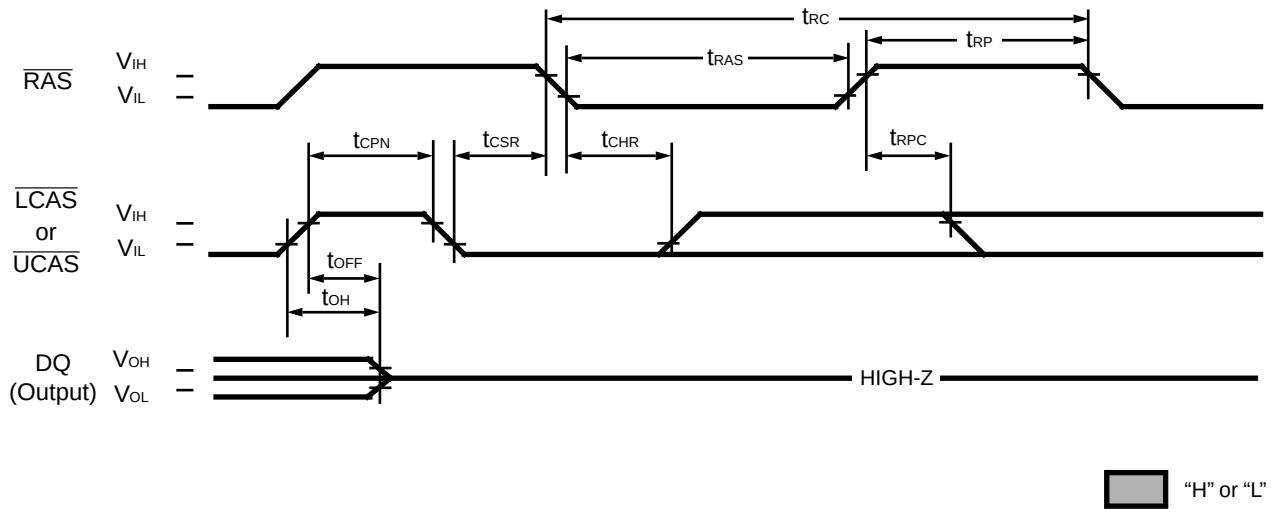



**DESCRIPTION**

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 4096 row addresses every 65.6-milliseconds. Three refresh modes are available: $\overline{RAS}$-only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$-only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{LCAS}$ and $\overline{UCAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$-only refresh, DQ pins are kept in a high-impedance state.

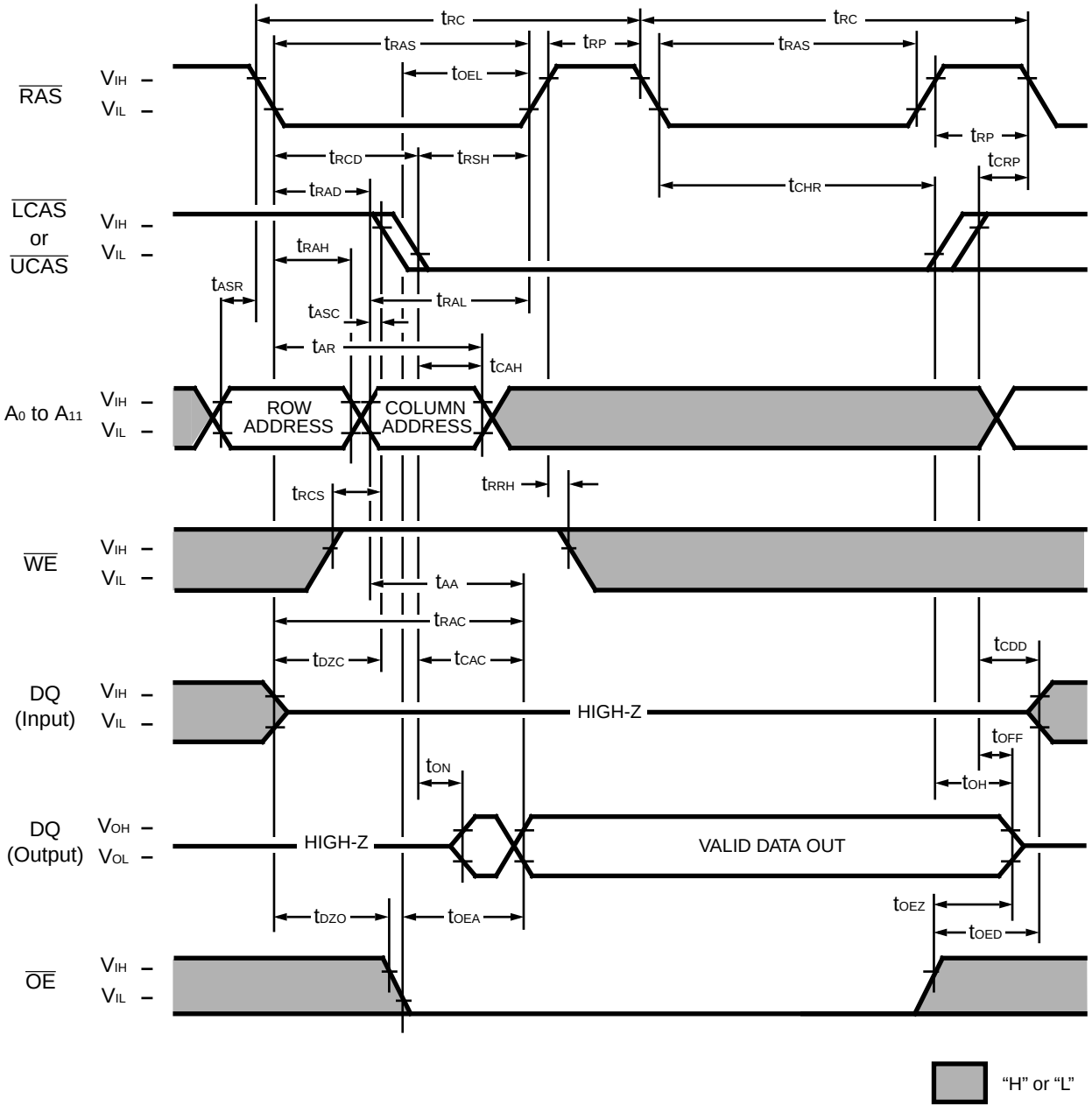
**Fig. 14 – $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH (ADDRESSES = $\overline{WE}$ = $\overline{OE}$ = "H" or "L")**




**DESCRIPTION**

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{LCAS}$ or $\overline{UCAS}$ is held Low for the specified setup time ($t_{CSR}$) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

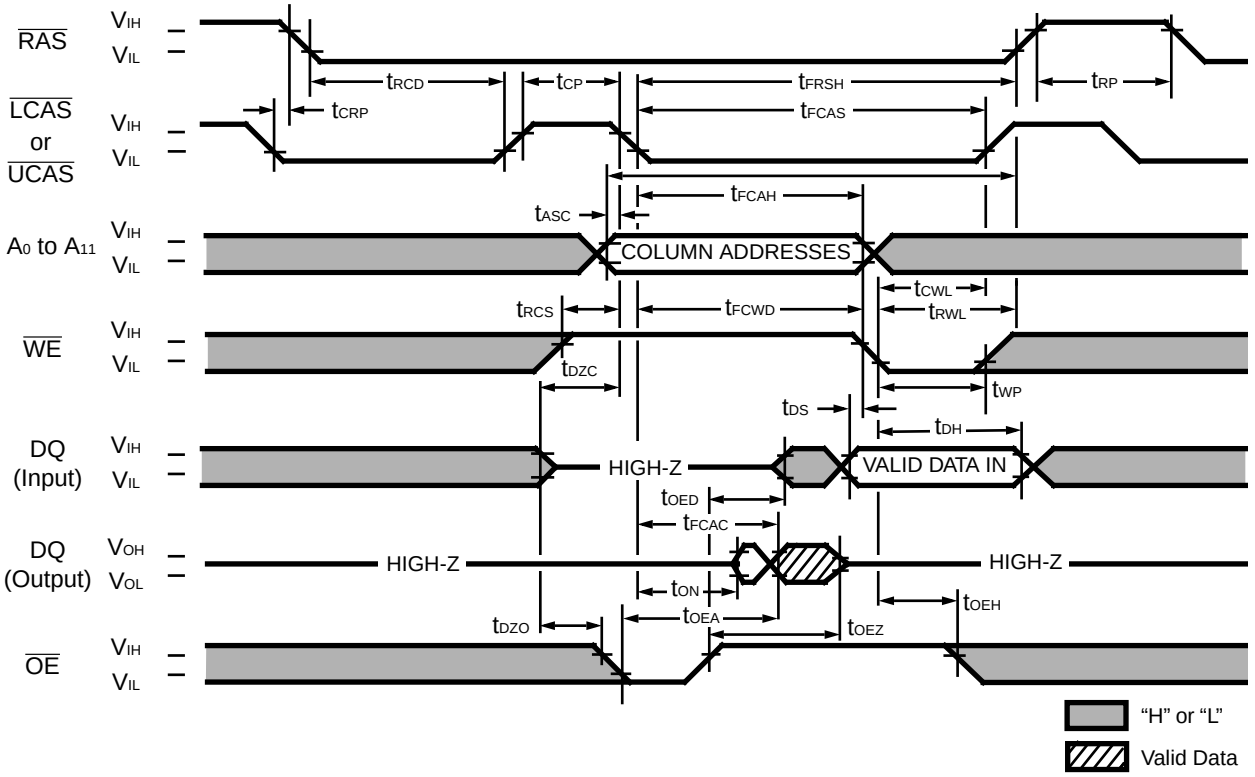
**Fig. 15 – HIDDEN REFRESH CYCLE**




**DESCRIPTION**

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ and cycling $\overline{\text{RAS}}$. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh capability.

**Fig. 16 – $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE**




**DESCRIPTION**

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method to verify the function of $\overline{CAS}$-before-$\overline{RAS}$ refresh circuitry. If, a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle $\overline{CAS}$ makes a transition from High to Low while $\overline{RAS}$ is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits A0 through A11 are defined by the on-chip refresh counter.
Column Address: Bits A0 through A7 are defined by latching levels on A0-A7 at the second falling edge of $\overline{CAS}$.

The $\overline{CAS}$-before-$\overline{RAS}$ Counter Test procedure is as follows ;

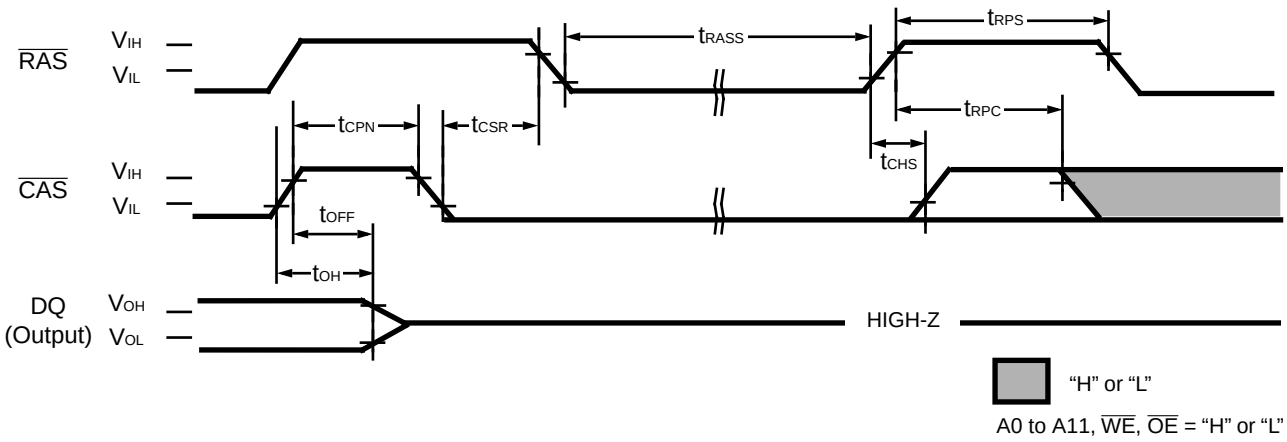
1) Initialize the internal refresh address counter by using 8 $\overline{RAS}$-only refresh cycles.
2) Use the same column address throughout the test.
3) Write "0" to all 4096 row addresses at the same column address by using normal write cycles.
4) Read "0" written in procedure 3) and check; simultaneously write "1" to the same addresses by using $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test (read-modify-write cycles). Repeat this procedure 4096 times with addresses generated by the internal refresh address counter.
5) Read and check data written in procedure 4) by using normal read cycle for all 4096 memory locations.
6) Reverse test data and repeat procedures 3), 4), and 5).

**(At recommended operating conditions unless otherwise noted.)**

| No. | Parameter | Symbol | MB8116160A-60 | | MB8116160A-70 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| 90 | Access Time from $\overline{CAS}$ | $t_{FCAC}$ | — | 50 | — | 55 | ns |
| 91 | Column Address Hold Time | $t_{FCAH}$ | 35 | — | 35 | — | ns |
| 92 | $\overline{CAS}$ to WE Delay Time | $t_{FCWD}$ | 70 | — | 77 | — | ns |
| 93 | $\overline{CAS}$ Pulse Width | $t_{FCAS}$ | 90 | — | 99 | — | ns |
| 94 | $\overline{RAS}$ Hold Time | $t_{FRSH}$ | 90 | — | 99 | — | ns |

Note: Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle only.

**Fig. 17 – SELF REFRESH CYCLE (A0-A11 = $\overline{WE}$ = $\overline{OE}$ = "H" or "L")**




**(At recommended operating conditions unless otherwise noted.)**

| No. | Parameter | Symbol | MB8116160A-60 | | MB8116160A-70 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| 100 | $\overline{CAS}$ Pulse Width | $t_{RASS}$ | 100 | — | 100 | — | µs |
| 101 | $\overline{RAS}$ Precharge Time | $t_{RPS}$ | 110 | — | 125 | — | ns |
| 102 | $\overline{CAS}$ Hold Time | $t_{CHS}$ | –50 | — | –50 | — | ns |

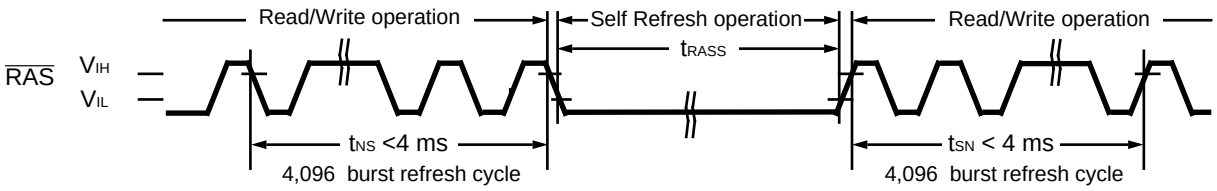
Note: Assumes self refresh cycle only

**DESCRIPTION**

The self refresh cycle provides a refresh operation without external clock and external Address. Self refresh control circuit on chip is operated in the self refresh cycle and refresh operation can be automatically executed using internal refresh address counter and timing generator. If $\overline{CAS}$ goes to "L" before $\overline{RAS}$ goes to "L" (CBR) and the condition of $\overline{CAS}$ "L" and $\overline{RAS}$ "L" is kept for term of $t_{RASS}$ (more than 100 µs), the device can enter the self refresh cycle. Following that, refresh operation is automatically executed at fixed intervals using internal refresh address counter during "$\overline{RAS}$ = L" and "$\overline{CAS}$ = L".
Exit from self refresh cycle is performed by togging $\overline{RAS}$ and $\overline{CAS}$ to "H" with specified $t_{CHS}$ min.. In this time, $\overline{RAS}$ must be kept "H" with specified $t_{RPS}$ min..
Using self refresh mode, data can be retained without external $\overline{CAS}$ signal during system is in standby.

Restriction for Self Refresh operation;
For self refresh operation, the notice below must be considered.

1) In the case that distributed CBR refresh are operated between read/write cycles
   Self refresh cycles can be executed without special rule if 4,096 cycles of distributed CBR refresh are executed within $t_{REF}$ max..
2) In the case that burst CBR refresh or distributed burst $\overline{RAS}$-only refresh are operated between read/write cycles
   4,096 times of burst CBR refresh or 4,096 times of burst $\overline{RAS}$-only refresh must be executed before and after Self refresh cycles.

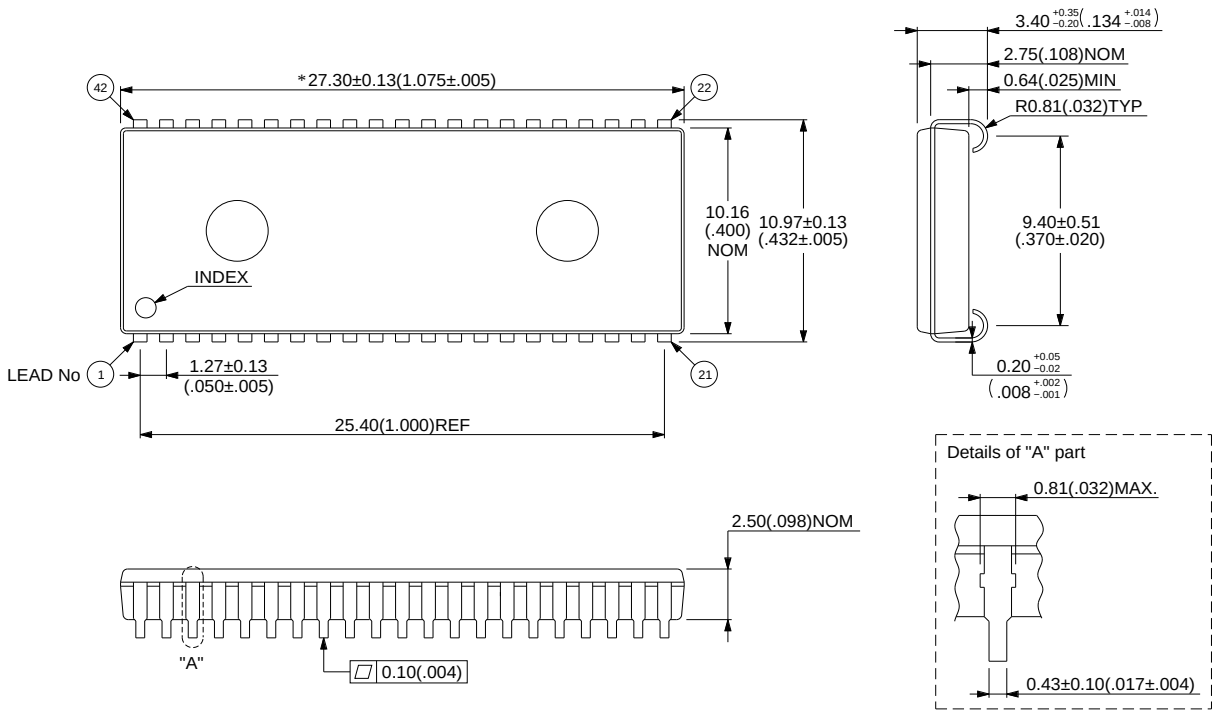



* read/write operation can be performed non refresh time within $t_{NS}$ or $t_{SN}$.

## ■ PACKAGE DIMENSIONS

(Suffix: -PJ)

42 pin, Plastic SOJ
(LCC-42P-M01)



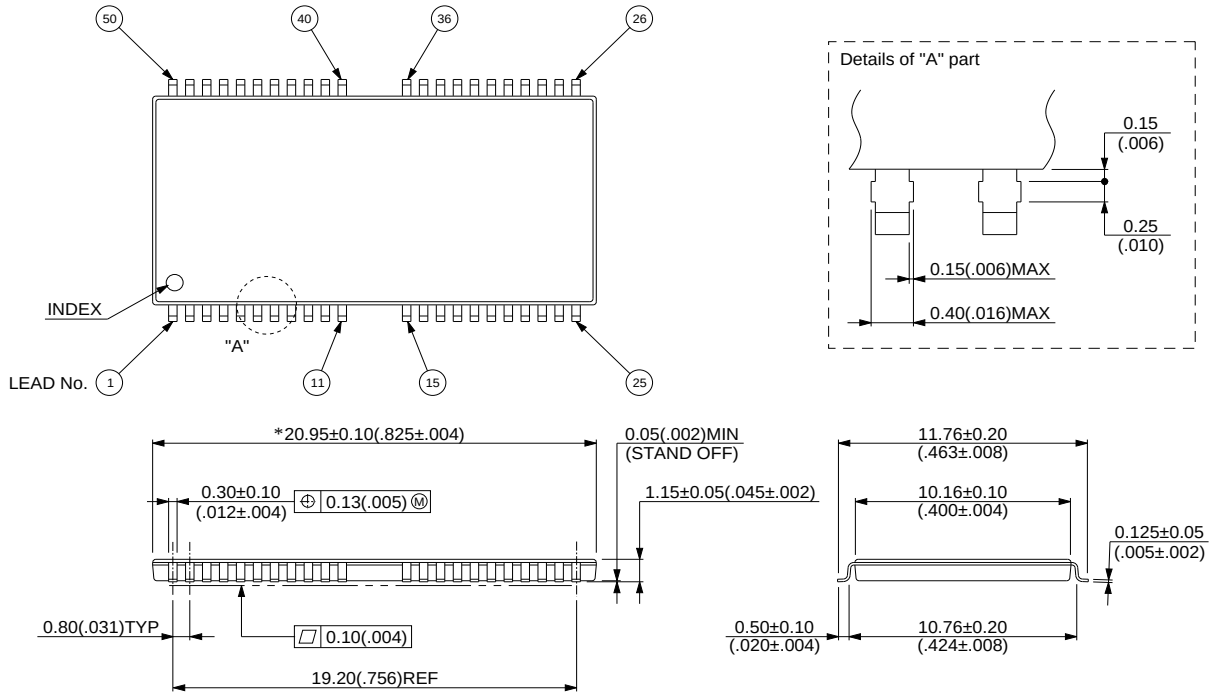



Dimensions in mm(inches).

## ■ PACKAGE DIMENSIONS (Continued)

(Suffix: -PFTN)

50 pin, Plastic TSOP(II)
(FPT-50P-M06)




Dimensions in mm(inches).

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